Abstract of the Disclosure:

A trench capacitor, in particular for use in a semiconductor memory cell, has a trench formed in a substrate; an insulation collar formed in an upper region of the trench; an optional buried plate in the substrate region serving as a first capacitor plate; a dielectric layer lining the lower region of the trench and the insulation collar as a capacitor dielectric; a conductive second filling material filled into the trench as a second capacitor plate; and a buried contact underneath the surface of the substrate. The substrate has, underneath its surface in the region of the buried contact, a doped region introduced by implantation, plasma doping and/or vapor phase deposition. A tunnel layer, in particular an oxide, nitride or oxinitride layer, is preferably formed at the interface of the buried contact. A method for producing a trench capacitor is also provided.

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